Professional Course Examination, November/December 2019

(5th Semester)

BACHELOR OF COMPUTER APPLICATIONS

Course : BCA–503

(Microprocessors)

Full Marks : 75

Time : 3 hours

(PART : A—OBJECTIVE)

(*Marks* : 25)

The figures in the margin indicate full marks for the questions

SECTION—A

(*Marks* : 15)

Tick (✓) the correct answer in the brackets provided : 1×10=10

1. In an Intel 8085, which is the first machine cycle of an instruction?

(a) An op-code fetch cycle ( )

(b) A memory read cycle ( )

(c) A memory write cycle ( )

(d) An I/O read cycle ( )

2. The numbers of output pins in 8085 microprocessors are

(a) 27 ( ) *(b)* 40 ( )

(c) 21 ( ) *(d)* 19 ( )

3. Temporary registers in 8085 are

(a) B and C ( ) *(b)* D and E ( )

(c) H and L ( ) *(d)* W and Z ( )

4. Which one of the following instructions can be used to clear the accumulator?
   (a) XRA A ( )
   (b) MVI A, OOH ( )
   (c) SUB A ( )
   (d) All of the above ( )

5. SIM stands for
   (a) Select Interrupt Mask ( )
   (b) Soring Interrupt Mask ( )
   (c) Set Interrupt Mask ( )
   (d) System Interrupt Mask ( )

6. The address bus of 8085 microprocessor is
   (a) 4-bit ( )
   (b) 16-bit ( )
   (c) 8-bit ( )
   (d) 32-bit ( )

7. The interrupt that has lowest priority is
   (a) TRAP ( )
   (b) RST 65 ( )
   (c) RST 7·5 ( )
   (d) INTR ( )

8. The length of SP (Stack Pointer) of 8085 microprocessor is
   (a) 8-bit ( )
   (b) 16-bit ( )
   (c) 12-bit ( )
   (d) 32-bit ( )

9. The _____ DAC internally converts the current signal into the voltage signal.
   (a) voltage output ( )
   (b) current output ( )
   (c) multiplying type ( )
   (d) All of the above ( )

10. The _____ is an 8-bit register that is part of the arithmetic and logical unit (ALU).

(a) stack pointer ( )

(b) accumulator ( )

(c) program counter ( )

(d) general purpose register ( )

Indicate whether the following statements are *True (T)* or *False (F)* by putting a Tick (✓) mark in the brackets provided : 1×5=5

1. An interrupt that can be turned off by the programmer is called maskable interrupt.

(T / F)

2. The 8085 instruction set includes Seven RST (Restart) instruction.

(T / F)

3. D/A converters are available as integrated circuit.

(T / F)

4. A time delay can be designed using a register pair.

(T / F)

5. TRAP is a maskable interrupt.

(T / F)

SECTION—B

(*Marks* : 10)

Answer the following questions : 2×5=10

1. What are the different logical operations available in 8085?

2. Differentiate between maskable and non-maskable interrupt.

3. What is DMA?

4. Explain data transfer operation.

5. Differentiate between encoder and decoder.

(PART : B—DESCRIPTIVE)

(*Marks* : 50)

The figures in the margin indicate full marks for the questions

1. *(a)* Draw and label the functional block diagram of 8085 microprocessor. 10

OR

(b) Explain the architecture of 8085 microprocessor and its operation with diagram. 7

(c) Explain the bus structure of 8085 microprocessor. 3

2. *(a)* Explain the 8085 microprocessor programming model with diagram. 6

(b) Differentiate between arithmetic operation and logical operation. 4

OR

(c) Define stack. Explain the operation of stack in detail. 5

(d) Explain the different types of addressing modes in 8085. 5

3. *(a)* What is time delay? Explain the time delay using a register pair. 5

(b) What are tri-state devices? Explain the circuit of tri-state buffer with diagram. 5

OR

(c) What is encoder? Explain the working of 8-to-3 lines encoder with diagram. 6

(d) Differentiate between latched flip-flop and clocked flip-flop. 4

4. *(a)* What is vectored interrupt? Explain the four types of vectored interrupt. 5

(b) Explain the maskable and non-maskable interrupt. 5

OR

(c) Explain the working of direct memory access (DMA) with diagram. 6

(d) Explain the function of IO/M, READY, HOLD and HLDA. 4

5. *(a)* Explain the working of analog-to-digital converter with block diagram. 5

(b) Explain successive approximation with diagram. 5

OR

(c) Explain the working of digital-to-analog converter with block diagram. 5

(d) Explain the working of R/2R ladder with diagram. 5

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